# PRADEEP CHAWDA

Pre-Silicon Design Quality & Reliability | Circuit Simulation | EDA | Design Enablement | Online Design Tools | Flows | Engineering Leadership

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## EXECUTIVE SUMMARY

Semiconductor engineering leader with 24+ years of experience across Apple, Texas Instruments, and National Semiconductor, leading engineering teams and developing circuit-simulation, EDA, design-automation, data, and MLOps platforms for analog and mixed-signal semiconductor design. Currently lead a Data and MLOps engineering team whose simulation platforms and designer-facing tools support hundreds of Apple Silicon engineers working on SERDES, PLLs, sensors, and complex IP. Earlier at Texas Instruments and National Semiconductor, developed pre-silicon signal-integrity and reliability tools including EM/IR analysis, voltage-level verification, static crosstalk analysis, and circuit simulation. Proven record of building tools adopted by 10K+ engineers worldwide; partnering with EDA vendors, leading distributed teams, and translating complex design requirements into scalable workflows that improve design quality and validation confidence.

## LEADERSHIP AND TECHNICAL EXPERTISE

- Pre-silicon design quality and reliability; validation and sign-off methodologies
- Circuit simulation: SPICE, Verilog-A, Verilog, compact device models, and behavioral modeling
- Signal integrity, power integrity, electromigration, IR drop, voltage-level verification, transistor aging, and floating-gate checks
- EDA tools, design automation, simulation orchestration, PCB design, data platforms, and CI/CD
- Global engineering leadership, organization design, resource allocation, operating metrics, and talent development
- Customer-facing technical platforms (Webench), designer workflows, cross-functional execution, and technology strategy

## PROFESSIONAL EXPERIENCE

### APPLE INC. | Engineering Manager, Apple Silicon Engineering

*February 2025 - Present | San Francisco Bay Area*

- Led a Data and MLOps engineering team whose software tools and simulation platforms serve hundreds of analog/mixed-signal designers building next-generation Apple SoCs, including SERDES, PLLs, sensors, and complex IP.
- Own multi-domain co-simulation frameworks bridging virtual prototyping, firmware, digital verification, and analog circuit simulation to enable whole-system reasoning before silicon exists.
- Direct data-platform engineering unifying simulation, lab, characterization, and factory data into pipelines supporting designer workflows and machine-learning models.
- Drive distributed orchestration for large-scale parallel simulation campaigns and apply ML, GenAI, agentic, and web-based tooling to improve design analysis and time to insight.
- Drove data adoption among 150+ engineers distributed across multiple locations in the U.S. and Europe.

### APPLE INC. | Architect, Analog and Mixed-Signal Software Development

*March 2019 - January 2025 | San Francisco Bay Area*

- Set architecture direction for core simulation, design-automation, and infrastructure serving Apple analog and mixed-signal design teams.
- Enabled internal mixed-signal simulation capabilities within industry-standard analog design environments; led distributed simulation orchestration for 100K+ simulation campaigns.
- Led Cadence and Synopsys vendor engagement to enable API-based co-simulation with the in-house simulator.
- Led ML-driven design-optimization tooling and initial deployment of an AMS data platform with hybrid storage, CLI/API/MCP, and dashboard integration.
- Owned DevOps and CI/CD evolution as the codebase and developer population grew tenfold; presented design-automation work at Apple engineering summits.
- Led a team of 20+ engineers distributed across Cupertino, Munich, Florida, San Diego, and Austin.

### TEXAS INSTRUMENTS | Lead Software Architect, WEBENCH Online Design Tools

*March 2016 - February 2019 | San Francisco Bay Area*

- Led platforms adopted by 100K+ engineers worldwide, including automated exchange between cloud-based design tools and offline simulation environments; enabled 80K+ design exports through the WEBENCH offline connector.
- Invented and delivered automated synthesis of multi-layer PCB coils for power and signal-chain applications; the tool was adopted by 10K+ users.
- Led development of an online PCB thermal-design tool using Node.js, Express, DevOps, and usage analytics to help customers predict TI product temperatures.
- Built customer-facing design tools and technical collateral connecting component selection, simulation, optimization, and export into downstream CAD environments.
- Led a team of 18 engineers distributed across Dallas, Bangalore, Hubli, Pune, Santa Clara and Canada.

**TEXAS INSTRUMENTS** | **Software Architect, WEBENCH Online Design Tools**

*September 2013 - February 2016 | San Francisco Bay Area*

- Architected Java Spring Boot REST APIs and an offline connector integrating WEBENCH designs with TINA-TI, Altium, OrCAD, and other CAD/simulation environments.
- Created design exchange and optimization workflows used by 40K+ customers, with 80K+ designs exported after release.
- Led a team of 15 engineers distributed across Dallas, Bangalore, Hubli and Santa Clara.

**TEXAS INSTRUMENTS** | **Principal Software Engineer, TIspice**

*October 2011 - August 2013 | Bengaluru, India*

- Led enhancement of TIspice for National Semiconductor IsSpice model simulation and replaced the commercial simulation engine inside WEBENCH with TIspice.
- Led a team of 12 engineers distributed across Bangalore, Dallas, and Santa Clara.

**NATIONAL SEMICONDUCTOR** | **Senior Staff Software Engineer, Custom Software Group**

*June 2009 - September 2011 | Bengaluru, India*

- Led cross-functional research and development of multi-domain behavioral modeling, simulation, and new-product concepts while guiding a team of 10 engineers.
- Proposed new product ideas with a three-year revenue potential of $100M; presented at National Semiconductor's Innovation Audition Conference in Silicon Valley in 2009 and 2010.

**NATIONAL SEMICONDUCTOR** | **Staff Software Engineer, Custom Software Group**

*October 2007 - May 2009 | Bengaluru, India*

- Led a six-engineer team developing an analog and mixed-signal circuit simulator supporting multiple SPICE syntaxes, Verilog-A, Verilog, and compact device models for system simulation.
- Defined and developed a layout-based resistance calculator, which was presented in CDNLive 2008 in Bangalore, India.

**TEXAS INSTRUMENTS** | **Senior Software Design Engineer, Mixed Signal Technology Center**

*July 2004 - August 2007 | Bengaluru, India*

- Defined, developed, and deployed signal-integrity and reliability tools for analog and mixed-signal designs, including VATIC, VOLTRACE, ANCOR, and SPIRE.
- Developed in-house signal and power EM/IR analysis; created pCell-based layout automation that reduced a triple-cascade amplifier layout cycle from approximately one week to a few minutes.
- Helped designers catch genuine violations before silicon and avoid silicon re-spin through automated voltage-level verification and static crosstalk analysis.
- Led a team of four engineers across Bangalore, Dallas, and France. Collaborated with two on-site Cadence application engineers on tool development.

## SELECTED INNOVATION

- Inventor/co-inventor on seven granted U.S. patents covering sensor design, power-converter compensation, circuit simulation, schematic generation, and design automation.
- Author/co-author of 15+ publications on IC design automation, circuit simulation, reliability, power management, and EDA; 100+ Google Scholar citations.
- Senior Member, IEEE; TI liaison to the Semiconductor Research Corporation's VLSI CAD/Machine Learning programs.

## AWARDS

- Nominated for the ISQED Best Paper Award, 2018.
- Best Presentation Award, CDNLive Silicon Valley, California, April 11-12, 2017.
- Winner of the Million-Dollar Idea Competition, Second Prize, National Semiconductor Innovation Conference, Santa Clara, CA, 2010
- Individual TI Recognition Awards for Best Execution in 2006, 2007, 2014, and 2015.
- Recognition Awards from National Semiconductor in 2009, 2010, and 2011.

## EDUCATION

M.Tech., Microelectronics and VLSI Design — Indian Institute of Technology, Bombay, 2004
B.E., Electrical Engineering — Chhattisgarh Institute of Technology, Bilaspur, 2002

## SELECTED TRAININGS

- Leadership Development — Apple University, 2025
- Generative AI and Agentic AI — Apple University, 2026

## SELECTED TOOLS AND TECHNOLOGIES

SPICE | Verilog-A | Verilog | EDA and design automation | EM/IR and signal integrity | Python | C/C++ | Java | Node.js | REST APIs | Distributed systems | Data engineering | MLOps | Machine learning | Snowflake | Altium Designer | Virtuoso | Allegro | Spectre